

PC Card Controllers

FEATURES

- A 253-Terminal MicroStar BGA Ball-Grid Array (GVF/ZVF) Package
- 2.5-V Core Logic and 3.3-V I/O with Universal PCI Interfaces Compatible with 3.3-V and 5-V PCI Signaling Environments
- Integrated Low-Dropout Voltage Regulator (LDO-VR) Eliminates the Need for an External 2.5-V Power Supply
- Mix-and-Match 5-V/3.3-V 16-Bit PC Cards and 3.3-V CardBus Cards
- A Single PC Card or CardBus Slot with Hot Insertion and Removal
- Parallel Interface to TI TPS2211A Single-Slot PC Card Power Switch
- Burst Transfers to Maximize Data Throughput with CardBus Cards
- Interrupt Configurations: Parallel PCI, Serialized PCI, Parallel ISA, and Serialized ISA
- Serial EEPROM Interface for Loading Subsystem ID, Subsystem Vendor ID, and other Configuration Registers
- Pipelined Architecture for Greater Than 130-Mbps Throughput from CardBus-to-PCI and from PCI-to-CardBus
- Up to Five General-Purpose I/Os
- Programmable Output Select for $\overline{\text{CLKRUN}}$
- Five PCI Memory Windows and Two I/O Windows Available for the 16-Bit Interface
- Two I/O Windows and Two Memory Windows Available to the CardBus Socket
- Exchangeable-Card-Architecture- (ExCA-) Compatible Registers Are Mapped in Memory and I/O Space
- Intel™ 82365SL-DF and 82365SL Register Compatible
- Ring Indicate, $\overline{\text{SUSPEND}}$, PCI $\overline{\text{CLKRUN}}$, and CardBus $\overline{\text{CCLKRUN}}$
- Socket Activity LED Terminal
- PCI Bus Lock ($\overline{\text{LOCK}}$)
- Internal Ring Oscillator

DESCRIPTION

The Texas Instruments PCI1510R device, a 144-terminal, 209-terminal, or 253-terminal single-slot CardBus controller designed to meet the *PCI Bus Power Management Interface Specification for PCI to CardBus Bridges*, is an ultralow-power high-performance PCI-to-CardBus controller that supports a single PC card socket compliant with the *PC Card Standard* (rev. 7.2). The controller provides features that make it the best choice for bridging between PCI and PC Cards in both notebook and desktop computers. The *PC Card Standard* retains the 16-bit PC Card specification defined in the *PCI Local Bus Specification* and defines the 32-bit PC Card, CardBus, capable of full 32-bit data transfers at 33 MHz. The controller supports both 16-bit and CardBus PC Cards, powered at 5 V or 3.3 V, as required.

The controller is compliant with the *PCI Local Bus Specification*, and its PCI interface can act as either a PCI master device or a PCI slave device. The PCI bus mastering is initiated during CardBus PC Card bridging transactions. The controller is also compliant with *PCI Bus Power Management Interface Specification* (rev. 1.1).

All card signals are internally buffered to allow hot insertion and removal without external buffering. The controller is register-compatible with the Intel 82365SL-DF and 82365SL ExCA controllers. The controller internal data path logic allows the host to access 8-, 16-, and 32-bit cards using full 32-bit PCI cycles for maximum performance. Independent buffering and a pipeline architecture provide an unsurpassed performance level with sustained bursting. The controller can also be programmed to accept fast posted writes to improve system-bus utilization.



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Multiple system-interrupt signaling options are provided, including parallel PCI, parallel ISA, serialized ISA, and serialized PCI. Furthermore, general-purpose inputs and outputs are provided for the board designer to implement sideband functions. Many other features designed into the controller, such as a socket activity light-emitting diode (LED) outputs, are discussed in detail throughout this document.

An advanced complementary metal-oxide semiconductor (CMOS) process achieves low system power consumption while operating at PCI clock rates up to 33 MHz. Several low-power modes enable the host power management system to further reduce power consumption.

NOTE:

This product is for high-volume PC applications only. For a complete datasheet or more information contact support@ti.com.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
PCI1510RGVF	OBSOLETE	NFBGA	GVF	253		TBD	Call TI	Level-3-220C-168 HR
PCI1510RZVF	OBSOLETE	NFBGA	ZVF	253		Pb-Free (RoHS)	SNAGCU	Level-3-250C-1 WEEK

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
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